

In re Patent Application of:
KASPER
Serial No. 10/758,379
Filing Date: January 15, 2004

REMARKS

Claims 18-47 remain in this application. Claims 1-17 have been cancelled. Claims 18-47 are previously presented. No claims have been amended.

Applicant thanks the Examiner for the detailed study of the application and prior art. Applicant notes that the transmittal cover sheet made the proper reference to the parent application, but in the present Amendment, Applicant amends the specification to include the reference to the prior application.

Also, Applicant submits a Terminal Disclaimer to overcome the double patenting rejection over U.S. Patent No. 6,691,178 corresponding to the issued parent application.

Also, Applicant notes the rejection of claims 18 and 19 as anticipated by U.S. Patent No. 6,182,164 to Williams and other claims as obvious over Williams in view of U.S. Patent No. 6,145,016 to Lai et al. (hereinafter "Lai"), or Williams in view of U.S. Patent No. 5,745,790 to Oskouy, or Williams in view of Oskouy, and further in view of Lai.

Applicant notes the allowable subject matter of claims 27, 32, 39 and 46.

At the outset, Applicant notes that the present invention is more than storing control and status data within a shared memory corresponding to different cache lines to minimize cache data processing overhead that appears to be how

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the Examiner views claim 18 and subsequent claims as defining the present invention.

The present invention reduces frame transfer latency in fencepost buffering procedures, which allows successive updating of spanned descriptors such that only terminal descriptors have to be altered. As a result, because of fencepost buffering, a packet can span a single descriptor, and at most two descriptors ever need to be updated. This relaxes the dependency between the packet size and buffer management overhead. The reduction of descriptor activity reduces total bus traffic and reduces packet latency. As a result, the present invention reduces transfer latencies in fencepost buffering in which first and second descriptor address locations are fed from a shared memory. The first descriptor address location is a location of an active descriptor, and the second descriptor address location is a location of a reserve descriptor. The active descriptor is copied to cache. It is at this time that a command is issued to a direct memory access unit (DMA) of the network controller for transferring the active descriptor back to the shared memory.

In accordance with one aspect of the invention, a next descriptor address location can be fetched from shared memory and placed in the second descriptor address location. It is also possible to update the ownership of terminal descriptors associated with the frame that are formed as end-

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of-frame (EOF) descriptors and start-of-packet (SOP) descriptors.

This is clearly set forth in claim 18 and its dependent claims. The other independent and dependent claims recite other aspects of the invention, including the updating and ownership of terminal descriptors and the chained descriptors, including end-of-frame (EOF) descriptors and start-of-packet (SOP) descriptors, and define terminal descriptors associated with the frame.

The Examiner has relied on Williams to allegedly disclose a method and system for reducing transfer latencies in fencepost buffering having chain descriptors. Applicant maintains that the Examiner has misinterpreted this cited reference. Williams is directed to a method and system for storing controlled data and status data in locations within a shared memory corresponding to different cache lines to minimize cache data processing overhead. There is no mention of chain descriptors, terminal descriptors, and the distinction between an active descriptor and a reserve descriptor or fencepost buffering.

Also, Applicant notes that Williams fails to disclose fetching first and second descriptor address locations from the shared memory wherein the first descriptor address location is a location of an active descriptor, and the second descriptor address location is a location of a reserve descriptor. Also, Williams fails to disclose copying

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the active descriptor to cache and issuing a command to a DMA unit of the network controller for a transfer of the active descriptor back to the shared memory.

Williams looks for cache hits and loads status data into cache from a shared memory. Thus, Williams is well able to store the status data and control data, but it is not directed to solving the problems as set forth in the present claimed invention.

The Examiner has also relied on Lai to disclose the use of a command issued to a network controller for transferring an active descriptor back to shared memory. Lai is directed to network interfacing and teaches the capability of a software driver to recognize the release of a descriptor back to the driver. There is no teaching of issuing a command to a network controller for the transfer of an active descriptor back to shared memory, much less the issuance of a command to the network controller for transfer of an active descriptor, stored in a cache between the controller and host, back to a shared memory as claimed.

As to Oskouy, it is directed to reporting data transfer between hardware and software in a computer system, including the use of "OWN" bits and descriptor rings. The Examiner notes that the end-of-frame descriptor of one packet will be written before the start-of-packet of a succeeding packet.

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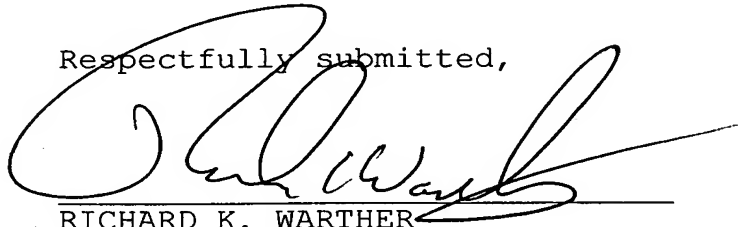
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Applicant notes that Oskouy does not mention chain descriptors, terminal descriptors, the distinction between an active descriptor and a reserve descriptor, or fencepost buffering as claimed. There is nothing in Oskouy to make up the deficiencies of Williams and Lai as discussed above.

It is clear that the present claimed invention is patentable over the cited references because those references do not singularly or in combination disclose or suggest the present claimed invention.

Accordingly, Applicant contends that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due. If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,



RICHARD K. WARTHER

Reg. No. 32,180

Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.

255 S. Orange Avenue, Suite 1401

Post Office Box 3791

Orlando, Florida 32802

Phone: 407-841-2330



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the full statutory term defined in 35 U.S.C. §154 to §156 and §173, and as the term of said prior patent is presently shortened by any terminal disclaimer, of U.S. Patent No. 6,691,178. Assignee hereby agrees that any patent so granted on the '379 Patent Application shall be enforceable only for and during such period that it and the '178 Patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the Grantee, its successors or assigns.

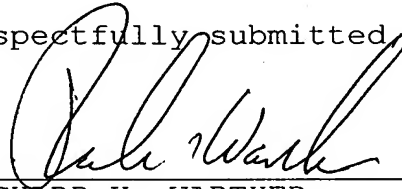
In making the above disclaimer, Assignee does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. §154 to §156 and §173 of the prior patent, as the term of said prior patent is presently shortened by any terminal disclaimer, in the event that it later expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. § 1.321, has all claims cancelled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term.

For submission on behalf of Assignee, the undersigned is the attorney of record.

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The Commissioner is hereby authorized to charge the terminal disclaimer fee in the amount of **\$130.00** to the credit card noted in the attached credit card payment form. If any additional extension and/or fee is required, charge Deposit Account No. **01-0484**.

Respectfully submitted,



RICHARD K. WARTHER
Reg. No. 32,180
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255-S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
Phone: 407-841-2330

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450**, on this 10th day of March, 2005.

